Calculation of Failure Rate of Semiconductor Devices Based on Mechanism Consistency

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Abstract Failure rate data of components is widely used in reliability design and analysis, such as reliability apportionment, reliability prediction, FMECA and so on. Currently, there are two major ways to evaluate failure rate: using prediction handbooks and accelerated life test. Updates to data in handbooks always are delayed, while accelerated life test costs lots of time and money, especially large-scale integrated circuits are expensive. In view of the defect, using corresponding test data provided by manufacturer's website to calculate failure rate is proposed based on failure mechanism consistency. Test data is analyzed and calculated to get failure rate of Semiconductor devices with each influencing mechanism, and values of failure rate under each mechanism are added together to get total failure rate based on the assumption of competition between mechanism.

1 Introduction

Failure rate of component is needed in reliability design and analysis, such as reliability apportionment, prediction, test, FMECA and so on. In electronic devices, the key components to achieve functions are mostly semiconductor devices. So, accurately estimating the failure rate of semiconductor devices is basis of proceeding reliability analysis accurately and effectively.

Now there are two ways commonly used in engineering to assess the failure rate of semiconductor devices. One is using prediction handbooks, such as MIL-STD-217F or GJB299C, which providing component failure rate data. Data update lag in handbooks cannot reflect the current semiconductor device design and manufacturing level very well. The other way is conducting accelerated life test, which accelerating components to fail by increasing the stress on the premise of the failure mechanism unchanged, then using model to calculate component life under practical conditions.

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Many scholars have done the research for accelerated life test [1] studied test stress type selection, determination of test conditions and so on [2, 3] studied accelerated test failure models. These studies have important theoretical and engineering value, and play a catalytic role for accelerated life applications in the field of reliability.

When the sample size is large, data obtained from accelerated life test is more accurate than using handbook. However, if we use accelerated life test to assess reliability of electronic products, accelerated test needed to be implemented for every component with long time and high cost, especially high cost of LSI chips.

Based on failure mechanism, this chapter provides a way to assess failure rate of semiconductor devices by analyzing existing experimental data under corresponding mechanism.

2 Related Theories

2.1 Failure Mechanism and Mechanism Consistency

Semiconductor devices mainly include wafer and package two parts in structure, so the failure rate can be divided into wafer failure rate and package failure rate to calculate. According to current research analysis, there are two types of component failure: time-related degradation and accidental failure. Due to impurities, process control and other factors, chip manufacturing defects will be caused in wafer fabrication, oxidation and photolithography process of semiconductor devices. These defects can induce various mechanism, such as metal key compounds, stress migration of metal wire inside the chip and so on, which is the root of dispersion. Studies [4, 5] show that semiconductor wafer failure can be considered to obey the exponential distribution in engineering, and the main environmental factor of affecting this failure is temperature. After the chip manufacturing, semiconductor devices are packaged to form complete devices. The main mechanism of package failure is crack propagation of lead bound interconnected parts, and its main factor is temperature cycling. Package failure is usually considered to obey two-parameter weibull distribution in engineering.

Accelerated life test should be taken in the premise that failure mechanism remains unchanged, that is to say, failure mechanism in accelerate tests is consistent with failure mechanism in field experiments. Experimental data is used to obtain the corresponding characteristic parameters of lifetime distribution, and then we can calculate the characteristic parameters of the product life distribution in true stress conditions according to the relationship between stress and life. Consistency between accelerated test data and field test data is important criteria of whether accelerated testing is successful. The key to implement test successfully is to explore the failure mechanism and its impact on product. Found in study, main failure mechanism of semiconductor device wafer is intermetallic compounds and metal wire stress migration, and the main environmental stress of affecting failure is steady temperature. Mechanism of semiconductor packaging is wire fatigue fracture

and the main environmental stress affecting the failure is temperature cycling. So semiconductor devices should be conducted accelerated test respectively with temperature and temperature cycling stress aiming at different mechanism.

2.2 Competition of Mechanism

For semiconductor devices having several kinds of mechanism, it is assumed that every failure mechanism is independent of each other when calculating characteristic parameters of the device lifetime distribution. Independent failure mechanism is not resulted from other mechanism in system but from the interaction between environmental conditions and internal factors. Every mechanism competes with each other, so series model is chosen to be reliability model of semiconductor devices.

Since every failure mechanism is resulted from the interaction between environmental conditions and internal factors, the impact of environmental conditions on the failure is reflected in the life distribution under the corresponding mechanism. We use accelerated test failure model which involves stress in test and reality to calculate acceleration factor, then calculate characteristic parameters in real life distribution combining with accelerated test data.

3 Approach to Analyze Test Data

According to the theory of failure mechanism consistency, HTOL test should be conducted for semiconductor device wafer failure, while temperature cycle test should be conducted for package failure. If failure rate of a variety of semiconductor devices is assessed by designing and implementing accelerated life test, it would cost a lot of money and time. At present, many large manufacturers make public a large number of experimental data. So these data could be screened according to the mechanism consistency. Then failure rate under the mechanism can be obtained by analyzing and calculating these data. For semiconductor devices, we can screen data to get appropriate data of the HTOL test and temperature cycling test to calculate failure rate of wafer failure and package failure. This chapter uses the reliability test database in ADI as an example to illustrate the way to assess semiconductor device failure rate by using existing reliability data.

3.1 Calculation of Failure Rate of Wafer

It is assumed that large electronic component manufacturers, such as Analog Devices, NS, AMD, hp, MAX, Texas, Toshiba, have considerable level of component control process during the same period, and wafers manufacturing with the

same process have consistent dispersion. For component manufactured in ADI, its wafer failure rate under specified operating temperature can be obtained directly from ADI reliability database. Analogy to similar products based on information of package, process and parameter could be used to assess failure data of component from other manufactures which is similar to component in ADI database.

Semiconductor wafer failure is considered to obey the exponential distribution. In no replacement censoring life test, lower confidence limit of average life product obeying exponential distribution in the confidence level of $1 - \alpha$ is:

$$\theta_L = \frac{2T}{\chi^2_{1-\alpha}(2r+2)} \tag{1}$$

In the equation, θ_L is the lower confidence limit of average life; χ^2 is Chi-square distribution, Value depending on the number of failures and confidence; T is total test time.

ADI's website provides data with no failure of censored time HTOL test. It is assumed that N is number of HTOL test samples; H is HTOL test duration and A_t is acceleration factor. So equivalent total test time is $T = N \cdot H \cdot At$, and χ^2 values $\chi^2_{1-\alpha}(2)$, for r = 0, confidence level is $1 - \alpha$. According to the Eq. (1), it can be launched expected failure rate of device wafer is:

$$\lambda = \frac{\chi^2_{1-\alpha}(2r+2)}{2T} = \frac{\chi^2_{1-\alpha}(2)}{2N \cdot H \cdot At} \tag{2}$$

In the equation, λ is expected failure rate of device wafer.

Addition to knowing the number of test samples, test time and the number of failure data, it is necessary to obtain the value of acceleration factor At in HTOL test to estimate expected failure rate of device wafer at a certain confidence level. Acceleration factor is calculated based on accelerated testing and field trials stress levels, describing the relationship between environmental stress and life distribution parameters.

3.2 Calculation of Failure Rate of Package

Semiconductor device forms a complete device through package after manufacturing chip. The main mechanism of package failure is crack propagation of lead bound interconnected parts, and the main factor affect the failure is temperature cycling. Package failure is usually considered to obey two-parameter weibull distribution in engineering. The key to calculate package failure rate is the calculation of package shape parameter β and scale parameter η.

ADI provides a wealth of temperature cycling test data of components in a variety of processes. Cycling condition is −65/+150 °C, etc. these reliability tests

are censored time, almost no failures. The approach to obtain β and η in failure probability density distribution by using these on failure data is described in the following.

3.2.1 Shape Parameter β

Currently, shape parameter data in fatigue Weibull distribution is already accumulated in engineering. Study [6] points that according to research from aviation sectors of United States, Britain, Japan and Australia and other countries, the limit of shape parameter in Weibull distribution which fatigue crack formation and propagation obeys for metal structure is approximately 2.2. Boeing's statistical analysis from lots of test data in Weibull distribution also show that, shape parameter in Weibull distribution of various metal structure fatigue fracture is in the range of about 2.2–4.0. In this chapter, the limit of the shape parameter β in Weibull distribution of crack propagation in lead bound interconnected parts is 2.2.

3.2.2 Scale Parameter η

After determining the shape parameter β based on engineering experience and historical data, test data with no failure is used to obtain product's characteristic life η. When the shape parameter is known, one-sided confidence limit of characteristic life η in Weibull distribution at confidence level of $1 - \alpha$ can be calculated by using the following equation:

$$\eta_L = \left[\frac{\sum_{i=1}^{n} t_i^{\beta}}{-\ln \alpha} \right]^{\frac{1}{\beta}} \tag{3}$$

Scale parameter η in Weibull distribution under different temperature cycling is different. As the changes of scale parameter η in Weibull distribution of wire fatigue fracture caused by different temperature cycling consistent with the inverse power-law relationship, Characteristic life η in real case can be calculated according to the inverse power-law relationship.

According the obtained shape parameter β and scale parameter η, package failure rate function can be achieved.

$$\lambda(t) = \frac{\beta}{\eta^{\beta}} t^{\beta - 1} \tag{4}$$

Then combined with the device operating time, the value of package failure rate can is worked out. Finally, failure rate of wafer and package are added to calculate the failure rate of semiconductor devices.

4 Calculation Example

In this section, Field effect transistor IRF5210 will serve as an example to describe the calculation method for failure rate of semiconductor devices. The package of IRF5210 is TO-220AB, and manufacturing process of its wafer is >2.5 μm^2 Bipolar.

Firstly, select its production process in the ADI database [7], and enter the working temperature 70 °C, then the failure rate of IRF5210 wafer at 70 °C can be given directly by running in the background as shown in Fig. 1.

The specific calculation method is calculating the acceleration factor A_t by using Arrhenius model based on the operating temperature and the test temperature. After knowing the acceleration factor A_t, failure rate of corresponding wafer could be work out by the Eq. 1 with appropriate HTOL test data in ADI database.

Arrhenius model equation is shown below:

$$A_t = \exp\left[\frac{E_a}{B}\left(\frac{1}{T_u} - \frac{1}{T_s}\right)\right] \tag{5}$$

In the equation, E_a is the activation energy; B is Boltzmann constant, value 0.00008623 eV/K; T_u is operating temperature; T_s is test temperature.

Then collect data with TO package and process >2.5 μm^2 Bipolar in temperature cycling test data provided in ADI's database, shown in Table 1.

Use Eq. (3) to calculate respectively the point estimates of the η under two different cyclic temperature. Generally, we choose confidence limit under the level "$1 - \alpha = 0.5$" as point estimate of characteristic life η. Then we calculate K and n based on the inverse power law equation combining with different temperature difference in cycling test and corresponding estimate of η. the inverse power law is shown in the following.

Fig. 1 Page of calculation of failure rate of wafer

Wafer Fabrication Data

Process Technology: >2.5um^2 Bipolar

>2.5um^2 Bipolar Life Test Data Summary	
Overall Sample Size	20028
Qty. Fail	0
Equivalent Device Hrs. @ 70 deg C)	763356016
FIT Rate (60% CL, 70 deg C)	1.2
MTTF (60% CL, 70 deg C)	833094343
FIT Rate (90% CL, 70 deg C)	3.02
MTTF (90% CL, 70 deg C)	331522039
Calculations assumes 0.7 eV Activation Energy	
To recalculate the summary table with a different operating temperature, enter a temperature and click Recalculate: 70 °C Recalculate	

Table 1 Cycling test data with TO package and process >2.5 μm^2 bipolar

Temperature cycling (°C)	Test time/h	Sample size	Number of failure
−65/+150	500	1,855	0
−65/+150	1,000	746	0
−40/+125	500	2,645	0
−40/+125	1,000	1,038	0

$$\eta = \frac{1}{K(\Delta T)^n} \tag{6}$$

After calculating K and n, we calculate η in the real working condition −40/70 °C by using the inverse power law. Then work out that failure rate of IRF5210 package is 4.2×10^{-9}/h based on Eq. (4) with working time 10 h.

Based on mechanism competition model, reliability model of semiconductor device is series model. So, failure rate of IRF5210 is obtained by add failure rate of wafer and package together. Finally, we calculate that failure rate of IRF5210 working 10 h is 7.2×10^{-9}/h.

5 Comparison with Failure Rate Assessment Method Based on Handbook

From the above results, failure rate of IRF5210 is conservative calculated as 7.2×10^{-9}/h based on test data provided by component manufacturers. While it is calculated as 1.62×10^{-8}/h through calculation method provided in Appendix A.2.3.2 of GJB299C.

The latest version of GJB/Z299C-2006 "Electronic Equipment Reliability Prediction Handbook" was released in 2006. In the past 7 years, the manufacturing process and quality of components improved and the failure rate significantly reduced. So, failure rate data in GJB299C might be too large to reflect the current level of component manufacturing.

Reliability prediction in database provided by Manufactures is based on test data, these data in database has been kept up to date. Therefore, these data can reflect the current level of design and manufacture of components. For example, data in ADI' website last updated on August 06, 2013. This method using the latest reliability data to calculate failure rate can be used engineering application.

6 Conclusion

This chapter first describes the major semiconductor device failure mechanisms; and then uses corresponding reliability test data provided by semiconductor device manufacturers to calculate failure rate of component under various mechanism based on mechanism consistency; finally, add failure rate of different mechanism together to get failure rate of semiconductor devices under the assumption that the mechanism competitive relationship.

Using these test data not only can save cost of test, and can reflect the current component design and manufacturing better than handbooks because these data have been kept up to date. The method calculating failure rate introduced in this chapter combines reliability data analysis knowledge with test data. If components have sufficient test data, this approach can be used in reliability prediction.

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